REMARKS

Examiner K. Chen is thanked for the thorough examination and search of the subject Patent Application. Claims 6, 8, 9, 11, 14-17, and 19-25 have been amended.

The Specification has been amended on pages 6-7 to correct a typographical error in the terms W and L. The Specification has been amended at pages 10-13 to correct the error noted by the Examiner where the buried strap was incorrectly referred to by the number 60. The Examiner is correct that it should be 62 as shown in the drawings. It is believed that this correction to the Specification overcomes the objection to the drawings.

Claims 6, 8, 9, 1, 14-17, and 19-25 have been amended to overcome rejection under 35 U.S.C. 112. The Examiner is thanked for his very helpful suggestions in this matter and especially for noticing the error in claim numbering.

All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1 and 6 as being anticipated by Heo et al is requested

in accordance with the following remarks.

It is a key feature of Applicants' invention that the buried strap is formed by a selective silicon deposition process. Claims 1 and 6 claim this selective deposition process, shown in Fig. 6. In the process described in Heo et al with reference to Fig. 1C, the polysilicon layer is deposited within the trench 112 where it is polished back by CMP (col. 1, lines 49-54) to form buried strap 122. Thus, Applicants' claimed selective deposition process is not disclosed in Heo et al.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 1 and 6 as being anticipated by Heo et al is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 2-5 and 7-25 as being unpatentable over Heo et al is requested in accordance with the following remarks.

As pointed out above, Heo et al does not disclose selective deposition of polysilicon. It is discussed on page 11 of the Specification that Applicants' process of selective polysilicon deposition deposits the buried strap to a controlled thickness that cannot be achieved by Heo's method

of non-selective deposition and CMP. Applicants' invention avoids CMP as taught on pages 11 and 13. Heo does not teach or suggest the key selective deposition to form the buried strap of Applicants' invention.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 2-5 and 7-25 as being unpatentable over Heo et al is requested in accordance with the remarks above.

Applicants have reviewed the prior art made of record and not relied upon, specifically Chakravarti et al and agree with the Examiner that while the reference is of general interest, it does not apply to the detailed Claims of the present invention. In particular, this reference also teaches a non-selective polysilicon deposition and CMP to form the buried strap.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Specification and Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Chen not find that the Claims are now Allowable that he call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph bridging pages 6-7 with the following:

Referring now more particularly to Fig. 1, there is shown a semiconductor substrate 10. Deep trench capacitor 24 has been formed partially underlying shallow trench isolation 28. Gate electrodes and interconnection lines 30 and bit lines 36 have been formed overlying the semiconductor substrate. Buried strap 40 forms diffusion junction 42. [W] L is the buried strap height defined by (recess 2 - recess 3) in the conventional scheme. [L] W is the buried strap width defined by the overlap between the deep trench and the active area. The junction depth of the buried strap diffusion junction 42 is a function of the buried strap height, temperature, and time during the post recess anneal step. Buried strap resistance is a function of the doping concentration of the second polysilicon layer, the buried strap junction depth, and buried strap width. It is desired to have a minimal buried strap resistance which defines drain sheet resistance.

Please replace the first full paragraph on page 10 through the top of page 12 with the following:

The preferred selective HSG polysilicon process will now be described. Preferably, the optional surface amorphization step by plasma doping has been performed to provide surface mobility of the silicon atoms in 54 to promote HSG formation. Now, selective HSG [60] 62 is formed as is conventional in the art for stacked capacitor applications.

The polysilicon [60] 62 (or other conductive layer) can be doped in-situ during or immediately after the deposition step. Alternatively, the polysilicon layer [60] 62 can be doped after deposition using plasma doping, plasma ion immersion implantation (PIII), or gas phase doping (GPD) for fine dose control. Fig. 7 illustrates the alternative post-deposition doping step 65. Doping (in-situ or post-deposition) uses arsenic or phosphorus ions for a doping concentration of between about 1E18 to 1E21 ions/cm^3.

The polysilicon layer [60] 62 formed by HSG has a thickness of between about 20 and 100 nm and a grain size of between about 10 and 50 nm. This HSG layer will form the buried strap of the present invention. The selective HSG

polysilicon deposition method deposits the buried strap polysilicon to a controlled thickness. This process avoids planarization of the buried strap layer by CMP which adds process complexity.

Optionally, a capping layer 64 may be formed over the buried strap [60] 62, as shown in Fig. 8. The optional capping layer 64 may be used to suppress dopant loss or to minimize the surface stress which might cause dislocation into the crystalline silicon substrate. A trench top oxide or other capping layer such as silicon nitride 64 may be deposited using a selective oxidation method or by an unbiased silicon nitride liner method, whichever is appropriate for a chosen integration method, to a thickness of between about 10 and 20 nm. This additional layer may serve as a sacrificial capping layer against any contamination during or after the integration steps such as annealing or implantation steps.

Please replace the first paragraph on page 13 with the following:

The silicon nitride layer 14 is stripped using a wet etching process. Now, a gate oxide layer 80 is grown on the substrate surface in the active area, as shown in Fig.

14. Gate electrodes 84 are formed as is conventional in the art. Buried strap diffusion junction 86 is formed by outdiffusion from the buried strap [60] 62 during thermal processes. The diffusion junction 86 provides a connection between the deep trench capacitor 54 and the transistor 84.

IN THE CLAIMS

Please amend the claims as follows:

6. (AMENDED) The method according to Claim 1 wherein said selective deposition layer is selected from the group [containing] consisting of: a hemispherical grain polysilicon layer, a SiGe layer, a polysilicon layer, and a pseudo-epitaxial silicon layer.

8. (AMENDED) The method according to Claim [8] 7 before said step of selectively depositing said hemispherical grain polysilicon layer further comprising plasma doping said silicon layer to amorphize a surface of said silicon layer.

9. (AMENDED) The method according to Claim [8] 7 wherein said step of selectively depositing said hemispherical grain polysilicon layer comprises in-situ doping of said

polysilicon layer.

11. (AMENDED) The method according to Claim [11] 10 wherein said doping step is selected from the group [containing] consisting of: plasma doping, plasma ion immersion implantation, and gas phase doping.

14. (AMENDED) The method according to Claim [14] 13 wherein said selective deposition layer is selected from the group [containing] consisting of: a hemispherical grain polysilicon layer, a SiGe layer, a polysilicon layer, and a pseudo-epitaxial silicon layer.

15. (AMENDED) The method according to Claim [14] 13 wherein said step of selectively depositing said layer comprises in-situ doping of said layer.

16. (AMENDED) The method according to Claim [14] 13 after said step of selectively depositing said layer further comprising doping said selective deposition layer to a concentration of between about 1E18 and 1E21 ions/cm^3.

17. (AMENDED) The method according to Claim [17] 16 wherein said doping step is selected from the group

[containing] consisting of: plasma doping, plasma ion immersion implantation, and gas phase doping.

19. (AMENDED) The method according to Claim [19] 18 wherein said step of forming said collar comprises:

growing or depositing an oxide layer within said deep trench; and

thermally densifying said oxide layer.

20. (AMENDED) The method according to Claim [19] 18 wherein said silicon layer comprises amorphous silicon.

21. (AMENDED) The method according to Claim [19] 18 wherein said selective deposition layer is selected from the group [containing] consisting of: a hemispherical grain polysilicon layer, a SiGe layer, a polysilicon layer, and a pseudo-epitaxial silicon layer.

22. (AMENDED) The method according to Claim [19] 18 wherein said step of doping said selective deposition layer is selected from the group [containing] consisting of: in-situ doping, plasma doping, plasma ion immersion implantation, and gas phase doping.

23. (AMENDED) The method according to Claim [19] 18 further comprising forming a capping layer overlying said selective deposition layer.

24. (AMENDED) The method according to Claim [24] 23 wherein said step of forming said capping layer is selected from the group [containing] consisting of: selective oxide deposition and silicon nitride deposition.

25. (AMENDED) The method according to Claim [16] 18 further comprising:

forming a shallow trench isolation region partially within said deep trench and said buried strap area; and

forming gate electrodes wherein said buried strap diffusion connects said deep trench capacitor to one of said gate electrodes to complete formation of said deep trench DRAM device.